[0066] First, as shown in **FIG. 8A**, a polycrystalline silicon film (not shown) is deposited on, for example, a p-type silicon semiconductor substrate **11** via a gate insulation film **12** by a CVD method or the like, and patterning of the polycrystalline silicon film and the gate insulation film **12** into an electrode shape causes to form a gate electrode **13**.

[0067] Next, as shown in **FIG. 8B**, side wall lower portions of the gate electrode **13** and a part of the gate insulation film **12** are removed by etching to make it notch-shaped. The notch sections become low permittivity regions **18**.

[0068] Next, as shown in **FIG. 8C**, ion implantation of an n-type impurity such as phosphorus (P) is performed using the gate electrode **13** as a mask, to form a pair of extension regions **16** on a surface layer of the semiconductor substrate **11**.

[0069] Next, as shown in **FIG. 8D**, a silicon oxide film (not shown) covering the gate electrode **13** and first films **14***a* is formed with low step coverage (low in step coverage) to such an extent as not to fill in the low permittivity regions **18**. This silicon oxide film may be formed by a low temperature oxidation (LTO) method or a sputtering method. For example, it is formed under the condition of low temperature of 400 by inputting high frequency (RF) power of 400 W with the use of a parallel plate plasma CVD apparatus. Then, full anisotropic etching (etch back) of this silicon oxide film causes to form sidewall films **19** that surround the low permittivity regions **18** being left as a cavity **24**.

[0070] Next, as shown in **FIG. 8E**, the ion implantation of the n-type impurity such as phosphorus (P) is performed using the gate electrode **13** and the sidewall films **19** as masks, and a source **17** and a drain **17** are formed on the surface layer of the semiconductor substrate **11** to partially overlap with the extension regions **16**.

[0071] Thereafter, interlayer insulation films, contact holes, various wiring layers, and the like are formed to bring the MOS transistor to completion.

[0072] Although the first to fourth embodiments exemplify a case to form a source and a drain in an LDD structure including an extension region, this invention is also applicable to a MOS transistor having only a single drain structure. In addition, this invention is not limited to a bulk-type MOS transistor and is also applicable to a MIS transistor, a SOI-type MOS transistor, a double gate type MOS transistor, and the like. Further, the low permittivity region may be provided not on both sides of the source and the drain but only on one side thereof.

[0073] Fringe Capacitance of MOS Transistor in the Present Embodiments

[0074] Here, taking the MOS transistor in the second embodiment (second aspect) for example, the relation between height of the low permittivity region (cavity) (which substantially corresponds to cavity size when width thereof is unified to a steady value (for example, 10 nm) and fringe capacitance is examined. **FIG. 9** shows a result of this simulation experiment.

[0075] In **FIG. 9**, the horizontal axis designates the height of the cavity, the left vertical axis designates the fringe capacitance, and the right vertical axis designates a relative value of fringe capacitance normalized by a value of a conventional device structure in which the cavity does not exist. As shown in the chart, locally forming a cavity of about 15 nm in height simply enables to reduce the fringe capacitance by 20 or more as compared to that of the conventional structure in which the cavity does not exist. Further, the similar simulation indicates that locally forming a microcavity having only 5 nm in height and 5 nm in width simply enables to reduce the fringe capacitance by 10 or more as compared to that of the conventional structure in which the cavity does not exist. In this case, even if the height of the cavity is further increased, great decrease in the fringe capacitance cannot be observed.

[0076] Therefore, as in this embodiment, the portion (side lower portion of the gate electrode) being the most effective in reducing the fringe capacitance is determined and then a required minimum cavity is locally formed in this portion, so that the fringe capacitance can be fully reduced with an impurity introduced in the gate electrode not escaping from the cavity in the heat treatment processes thereafter, which differs from the invention of Japanese Patent Laid-open No. Hei 9-246544. Note that this effect can be seen not only in the second embodiment but also in the first, third, and fourth embodiments.

[0077] According to the present invention, such a semiconductor device is realized as to reduce the fringe capacitance in the most effective manner and to deter an escape of the above-mentioned impurity as much as possible, as well as to have a relatively simple manufacturing.

[0078] The present embodiments are to be considered in all respects as illustrative and no restrictive, and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein. The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof.

[0079] Hereinafter, various aspects of this invention are described as claims.

1. A semiconductor device including a gate having a gate insulation film and a gate electrode, a source, and a drain, said semiconductor device comprising:

a sidewall film covering a side surface of said gate; and

a low permittivity region locally provided at a lower portion of the side surface of said gate with the low permittivity region being covered by said sidewall film,

wherein said gate insulation film and a lower end of said gate electrode have a same width as each other.

2. The semiconductor device according to claim 1, wherein said low permittivity region is made of a lower permittivity material as compared to said sidewall film.

3. The semiconductor device according to claim 2, wherein said sidewall film includes

a first film directly formed at an upper portion of said side surface of said gate, and

a second film formed on said first film to cover said low permittivity region directly formed at the lower portion of the side surface of said gate.

4. The semiconductor device according to claim 1, wherein said low permittivity region is a cavity.